

FROM McANDREWS, HELD, & MALLOY

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OCT 18 2006

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Docket No. 13435US04

### In the Application of:

M.F. Afghahi et al.

U.S. Serial No.: 10/795,825

Filed: March 8, 2004

**For: SINGLE-ENDED SENSE AMPLIFIER  
WITH SAMPLE-AND-HOLD  
REFERENCE**

Examiner: K.B. Wells

Group Art Unit: 2816

Confirmation No.: 2778

## **CERTIFICATE OF TRANSMISSION**

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, at (571) 273-8300 on October 18, 2006.

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## **BRIEF ON APPEAL**

MAIL STOP: APPEAL BRIEF-PATENTS  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

This is an appeal from an Office Action dated April 18, 2006, in which claims 1 and 5-8 were finally rejected.

## **REAL PARTY IN INTEREST**

Broadcom Corporation, a corporation organized under the laws of the state of California, and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment submitted for recordal on September 4, 2001, in parent application 09/712,422.

PAGE 717 \* RCVD AT 10/18/2006 9:22:58 PM [Eastern Daylight Time] \* SVR:USPTO-EFXRF-6/43 \* DNI:2738300 \* CSID:3127079155 \* DURATION (mm:ss):04-02

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**RELATED APPEALS AND INTERFERENCES**

There currently are no appeals pending regarding related applications.

**STATUS OF THE CLAIMS**

Claims 1 and 5-8 are pending in the present application. Claims 2-4 are cancelled. Pending claims 1 and 5-8 stand rejected and are the subject of this appeal.

**STATUS OF THE AMENDMENTS**

There are no amendments pending in the present application.

**SUMMARY OF CLAIMED SUBJECT MATTER**

Claim 1 is directed to a sense amplifier comprising a sampling circuit, a reference node and a timing circuit. The sampling circuit receives an input signal to the sense amplifier. The reference node stores a reference signal corresponding to the input data. The reference signal serves as a reference voltage of the sense amplifier. The timing circuit activates the sampling circuit a predetermined interval before measurement of the input signal is initiated, the sampling circuit admitting the input signal to the reference node thereby.

The invention of claim 1 is described in the Specification of the present application at, for example, pages 33, line 25 - page 34, line 23, referring to Figure 10. FIG. 10 illustrates a single-ended sense amplifier 1000 with a sample-and-hold reference.<sup>1</sup> FIG. 10 shows a sampling circuit comprising the transistor (unnumbered) that receives the input signal DataIn 1004.<sup>2</sup> A reference node 1021 stores a reference signal corresponding to the input data. The reference signal serves as a reference voltage of the sense amplifier.<sup>3</sup> The timing circuit activates the sampling circuit a predetermined

<sup>1</sup> Specification, page 33, lines 29-31.

<sup>2</sup> Specification, page 33, lines 32-34.

<sup>3</sup> Specification, page 34, lines 10-15.

interval before measurement of the input signal is initiated, the sampling circuit admitting the input signal to the reference node thereby.<sup>4</sup>

Claim 5 is directed to a method of sensing input data. Pursuant to the method, an input signal is received at a sense amplifier. The input signal is admitted to a reference node of the sense amplifier a predetermined interval before measurement of the input signal is initiated by the sense amplifier. The input signal admitted to the reference node is stored as a reference signal of the sense amplifier.

The invention of claim 5 is described in the Specification of the present application at, for example, pages 33, line 25 - page 34, line 23, referring to Figure 10. FIG. 10 illustrates a single-ended sense amplifier 1000 with a sample-and-hold reference.<sup>5</sup> FIG. 10 shows a sampling circuit comprising the transistor (unnumbered) that receives the input signal DataIn 1004.<sup>6</sup> A reference node 1021 stores a reference signal corresponding to the input data. The reference signal serves as a reference voltage of the sense amplifier.<sup>7</sup> The timing circuit activates the sampling circuit a predetermined interval before measurement of the input signal is initiated, the sampling circuit admitting the input signal to the reference node thereby.<sup>8</sup>

Claims 6-8 are dependent upon claim 5.

#### GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1 and 5-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,343,428 issued to Harold Pilo, et al.

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<sup>4</sup> Specification, page 33, lines 32-34, and page 34, lines 6-15.

<sup>5</sup> Specification, page 33, lines 29-31.

<sup>6</sup> Specification, page 33, lines 32-34.

<sup>7</sup> Specification, page 34, lines 10-15.

<sup>8</sup> Specification, page 33, lines 32-34, and page 34, lines 6-15.

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## ARGUMENT

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**Claims 1 and 5-8 are not anticipated under 35 U.S.C. § 102(b) by Pilo (US 5,343,428).**

In the Office Action of April 18, 2006, claims 1 and 5-8 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nagano (US 5,408,199). 35 U.S.C. 102(e) states:

A person shall be entitled to a patent unless... the invention was patented or described in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States.

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."<sup>9</sup>

Claim 1 is directed to:

1. A sense amplifier, comprising:  
a sampling circuit receiving an input signal to the sense amplifier;  
a reference node operable to store a reference signal corresponding to the input data, the reference signal serving as a reference voltage of the sense amplifier;  
a timing circuit activating the sampling circuit a predetermined interval before measurement of the input signal is initiated, the sampling circuit admitting the input signal to the reference node thereby.

In Item 3 of the Office Action dated December 1, 2005, the Examiner asserts that the "reference node" of claim 1 "reads on either node 102." Appellant assumes that the Examiner intended to assert that the reference node reads on either node 101 or 102 of Pilo. Appellant respectfully disagrees with this assertion. Nodes 101 and 102 of Pilo are not reference nodes of the sense amplifier 20, operable to store a reference signal. The terms "reference node," "reference signal" and "reference voltage" are terms of art that are well understood by those of skill in the art of sensing amplifiers as referring to a reference point to which a single-ended input signal is compared. Furthermore, claim 1 clarifies that "the reference signal serv(es) as a reference voltage of the sense amplifier." In the Office Action dated May 3, 2005, the Examiner argues that nodes 101 and 102 of Pilo are reference nodes "because they are performing the same function/operation as

applicant's 'reference' nodes, i.e., if applicant's node 1021 is a reference node, then so too is node 101 (or 102) of Pilo.<sup>10</sup> Appellant respectfully submits that nodes 101 and 102 of Pilo do not, in fact, perform the same function/operation as the reference node of claim 1 or reference node 1021 in FIG. 10. Specifically, nodes 101 and 102 do not function to store a reference voltage of the sense amplifier 20. In fact, the sense amplifier 20 of Pilo is a differential amplifier, as opposed to a single-ended amplifier. The sense amplifier 20 of Pilo senses the difference between complementary data input signals MUXLAT and MUXLAT\*, using differential amplifier 25.<sup>11</sup> Because the sense amplifier 20 of Pilo is a *differential* amplifier, it does not make use of a reference voltage at all. The nodes 101 and 102 of Pilo are not reference nodes, but rather are the nodes via which the complementary input signals MUXLAT and MUXLAT\* are inputted to the differential amplifier 25, or, alternatively, stored in latch 35.<sup>12</sup> Similarly, the "sampling circuit" of Pilo does not admit the input signal (MUXLAT or MUXLAT\*) to a reference node. Therefore, Appellant submits that claim 1 is not anticipated by Pilo.

In the Final Office Action, dated April 18, 2006, the Examiner responded to the above argument by saying, "in Pilo et al., charge is clearly stored at these nodes due to the action of capacitors 56 and 57."<sup>13</sup> This does not address the Appellant's argument. The fact that nodes 101 and 102 of Pilo store charge does not make either of them a reference node operable to store a reference signal that serves as a reference voltage of the sense amplifier.

The Examiner further responded to the arguments presented above by saying that "applicant's amplifier is also a differential amplifier, and therefore the Examiner sees no distinction."<sup>14</sup> Appellant submits that the sense amplifier of claim 1 and supporting disclosure (Figure 10) is not, in fact, a differential amplifier, but, conversely, a single-ended amplifier. See, e.g., page 33, lines 28-31 of the specification, stating, "FIG. 10 illustrates a single-ended sense amplifier 1000". The Examiner may be confused by FIG. 10's inclusion of a differential amplifier 1012. However, the data sensing functionality

<sup>9</sup> *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

<sup>10</sup> Office Action dated May 3, 2005, page 2, item 4.

<sup>11</sup> See, e.g., Pilo, et al., US Patent 5,343,428, col. 5, lines 12-16

<sup>12</sup> *Id.*

<sup>13</sup> Office Action dated April 18, 2006, page 2, item 4.

of the single-ended sense amplifier 1000 is performed not by the differential amplifier 1012, but rather is performed in a single-ended fashion, that is, via comparison of a single input signal 1004 to a reference voltage stored at reference node 1021.

In Item 3 of the December 1, 2005, Office Action, the Examiner asserts that the "timing circuit" of claim 1 "reads on the (unillustrated) circuitry which outputs the clock signal CLK." The timing circuit of claim 1 "activat(es) the sampling circuit a predetermined interval before measurement of the input signal is initiated, the sampling circuit admitting the input signal to the reference node thereby." The Examiner alleges that the circuitry in Pilo that outputs the clock signal CLK "activates the sampling circuit prior to measurement of the input signal MUXLAT."<sup>15</sup> Appellant disagrees with this statement; but more importantly, the statement mischaracterizes claim 1. Claim 1 states that the timing circuit "activat(es) the sampling circuit a predetermined interval before measurement of the input signal *is initiated*," as opposed to activating the sampling circuit a predetermined interval before measurement of the input signal *is completed*. Appellant submits that it is precisely the CLK signal of Pilo that initiates the measurement of the input signal.<sup>16</sup> Therefore, the CLK signal of Pilo cannot be said to activate the sampling circuit (consisting of inverters 36, 37 and 38 and transmission gates 40, 43 and 52) *a predetermined time before* measurement of the input signal *is initiated*. Put another way, in Pilo, activating the sampling circuit and initiating the measurement of the input signal are one and the same, and therefore the CLK signal of Pilo cannot activate the sampling circuit a predetermined time before measurement of the input signal is initiated.

Referring to FIG. 2 and column 7, lines 51-60, of Pilo, the transition of the CLK signal from low to high at time t4 causes the transfer gates 43 and 52 (the "sampling circuit") to become conductive, allowing the input signals MUXLAT and MUXLAT\* to propagate through the sense amplifier 20, as indicated by the successive transitions of the voltage levels of node 101, node 102, node 103, node 104 and output signals PED and PED\* after time t4. Thus, the transition of the CLK signal from low to high activates the sampling circuit and initiates the measurement of the input signals. It is the transition of

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<sup>14</sup> *Id.*

<sup>15</sup> Office Action dated December 1, 2005, page 2, item 3.

<sup>16</sup> See, e.g., Pilo, col. 5, lines 12-16 and col. 7, lines 51-60.

the CLK signal from low to high that causes the input signals MUXLAT and MUXLAT\* to be admitted to the differential amplifier 25, as indicated by the transitions of the voltage levels of node 101, node 102, node 103, node 104 and output signals PED and PED\* after time t4. Of course, the value of the output signals PED and PED\* do not change instantaneously upon the CLK transition (though nearly so); the propagation of the signal through nodes 101 and 102, and then through nodes 103 and 104, takes a finite (though very small) amount of time. But claim 1 says that the timing circuit activates the sampling circuit "a predetermined interval before measurement of the input signal is *initiated*," as opposed to "a predetermined interval before measurement of the input signal is *completed*." In Pilo, the activation of the "sampling circuit" (transfer gates 43 and 52) and the initiation of the measurement of the input signal are one and the same. Therefore, the timing circuit clearly does not activate the sampling circuit a predetermined interval before measurement of the input signal is initiated, as called for in claim 1. Thus Applicant submits that claim 1 further differentiates over Pilo.

In the Final Office Action, the Examiner responded to the above argument by saying, "The transmission gates 40, 43 and 52 of Pilo et al clearly must be activated prior to allowing the input signals to pass through to the sense amplifier so that the sense amplifier can (at a later point in time) perform the measurement of the input signal (i.e., the differential sensing operation)."<sup>17</sup> In response to this argument, Appellant submits that the measurement of the input signals of Pilo is initiated when the CLK signal activates the transmission gates 40, 43 and 52.<sup>18</sup> Therefore, the CLK signal of Pilo cannot be said to activate the sampling circuit (transmission gates 40, 43 and 52) *a predetermined time before* measurement of the input signal is *initiated*, as in claim 1.

Appellant notes that, in the Final Office Action, the Examiner responded to the Appellant's claim that the Examiner mischaracterized the timing circuit of claim 1, saying, "This argument makes no sense because the limitation now being argued was not even present in the previous claims, and therefore it makes no sense to argue that the examiner 'mischaracterized' a limitation that did not even exist at the time the rejection was made."<sup>19</sup> In response, Appellant would point out that claim 1 was amended into its

<sup>17</sup> Office Action dated April 18, 2006, page 2, item 4.

<sup>18</sup> See, e.g., Pilo, col. 5, lines 12-16 and col. 7, lines 51-60.

<sup>19</sup> Office Action dated April 18, 2006, page 2, item 4.

present form on November 3, 2005 and that the Examiner's mischaracterization of the timing circuit was in the Office Action dated December 1, 2005<sup>20</sup>, after claim 1 was placed in its present form. This point is of no substantive import, but Appellant wanted to respond to the Examiner's accusation.

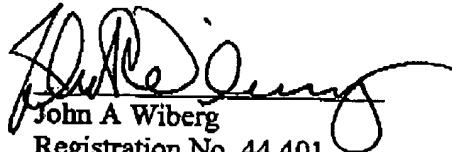
Claim 5 is similar to claim 1 and was rejected under the same grounds as claim 1. Therefore, Appellant submits that claim 5, and claims 6-8 depending therefrom, are not anticipated by Pilo for at least the reasons set forth above with respect to claim 1.

For at least the foregoing reasons, Applicant respectfully submits that claim 1 and 5-8 are allowable. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: October 18, 2006

Respectfully submitted,



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<sup>20</sup> Office Action dated December 1, 2005, page 2, item 3.

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The following claims are involved in this appeal:

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1. A sense amplifier, comprising:  
a sampling circuit receiving an input signal to the sense amplifier;  
a reference node operable to store a reference signal corresponding to the input data, the reference signal serving as a reference voltage of the sense amplifier;  
a timing circuit activating the sampling circuit a predetermined interval before measurement of the input signal is initiated, the sampling circuit admitting the input signal to the reference node thereby.
  
5. A method of sensing input data comprising:  
receiving an input signal to a sense amplifier;  
admitting the input signal to a reference node of the sense amplifier a predetermined interval before measurement of the input signal is initiated by the sense amplifier; and  
storing the input signal admitted to the reference node as a reference signal of the sense amplifier.
  
6. The method of claim 5 wherein receiving an input signal comprises receiving the input signal at a sampling circuit.
  
7. The method of claim 6 wherein admitting the input signal to a reference node comprises activating the sampling circuit a predetermined interval before measurement of the input signal is initiated by the sense amplifier.
  
8. The method of claim 5 further comprising measuring the input signal the predetermined interval after admitting the input signal to the reference node.

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**EVIDENCE APPENDIX (37 C.F.R. § 41.37(c)(1)(ix))**

None.

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**RELATED PROCEEDINGS APPENDIX (37 C.F.R. § 41.37(c)(1)(x))**

None.